

Short Communication

LOW POWER SI-BASED POWER AMPLIFIER FOR HEALTHCARE APPLICATION

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ABSTRACT

Objective: The objective of this research was to design a 2.4 GHz class B Power Amplifier (PA), with 0.18um Semiconductor Manufacturing International Corporation (SMIC) CMOS technology by using Cadence software, for health care applications. The ultimate goal for such application is to minimize the trade-offs between performance and cost, and between performance and low power consumption design.

Methods: This paper introduces the design of a 2.4GHz class B power amplifier designed as dual gate topology. This class B power amplifier could transmit 26dBm output power to a 50 load . The power added efficiency was 60 % minimum and the power gain was 90dB, the total power consumption was 6.9 mW.

Results: Besides, accurate device modeling, is needed, due to the leakage and process variations.

Conclusion: The performance of the power amplifier meets the specification requirements of the desired.

Keywords: Dual gate, Class B, Power amplifier

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Wireless medical sensor networks have offered significant improvements to the healthcare industry in the 21st century [1-2]. Devices are arranged on a patient's body and can be used to monitor the physiological condition of patients closely. These medical sensors monitor the patient's vital body parameters, such as temperature, heart rate, blood pressure, oxygen saturation, and transmit the data to a doctor in real time [1, 3-6]. When a doctor reviews the transmitted sensor readings, they can get a better understanding of a patient's health conditions. The benefit for the

patients is that they do not need to visit the hospital frequently, thus patients could reap time and money savings. Such wireless medical sensors will continue to play a central role in the future of modern healthcare. People living in rural areas would especially benefit since 9% of physicians work in rural areas while almost 20% of the US population lives there [2]. A shortage of physicians and specialist is a big issue in such areas, even today. But wireless medical sensor network technology has the potential to alleviate the problem.

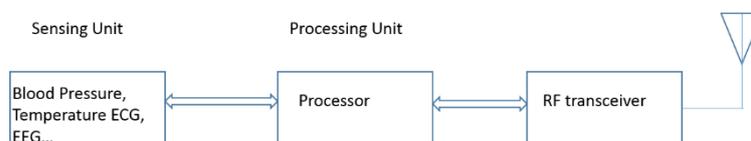


Fig. 1: Block diagram of a typical sensor node

In a wireless sensor network, as seen in the fig. 1 below, each device is capable of monitoring, sensing, and/or displaying information. A sensor node is capable of gathering sensory information, processing it in some manner, and communicating with other nodes in the network [7-10].

Fig. 1 shows that the basic sensing node can collect the physiological signals (e. g.: such as EEG, ECG, body temperature, blood pressure, heartbeat etc.), when attached to a human body [11]. The processing

unit processes all the sensed signals, then sends out the data based on communication protocols. All the processed data will be transmitted through a wireless link to a portable, personal base station. Doctors can then obtain all the patients' data through the network.

The main challenge for such sensor node is the high power consumption of portable devices. A solution to this challenge is the integration of the portable devices' digital and RF circuitry into one chip.

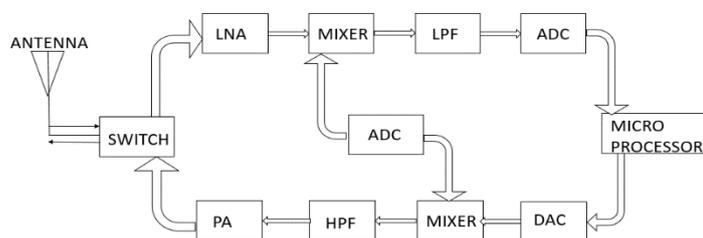


Fig. 2: Block diagram of a transmitter

The receiver will receive the signal and will also perform DSP processing after the data is sent out by the transmitter [11]. Fig. 2 is the transmitter diagram. It is desirable that the transmitter and receiver are low power devices. The direct-conversion transmitter is very popular for such applications because it offers versatility, flexibility, spectral efficiency, and low complexity. These features make the transmitter simpler than the super-heterodyne transmitter. Small chip and circuit size, and low

power consumption can be achieved with a direct-conversion transmitter architecture. For the front-end transmitter, the major objectives are 1) transmit RF signals and 2) recover the biosignal classification. This paper proposes a low power receiver design. This paper is mainly for the power amplifier design since other portions of the circuit design are already discussed in the paper [11]. In order to meet the standards, the PA is designed as shown in table 1.

Table 1: PA design requirement

Parameter	Size (Unit)
Power Gain	50 dBm
PAE	50%
Stability	>1
Output Power	20 dB

Over the past 30 y, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost and between performance and low power consumption design [11].

The proposed Class B amplifier has low output power and good linearity based on the IEEE 802.11b communication protocol. The class B power amplifier topology is shown in fig. 3.

To ensure low cost, so the PA is designed via a CMOS process. And the initial requirements as seen in table 1.

This paper examines a single-ended, class B power amplifier with a low-pass filter. This singled ended class B power amplifier design simultaneously achieves high power added efficiency (PAE) and high third-order intermodulation (IM3) suppression.

The added filter can block unwanted frequencies during Class B operation. The Class B power amplifier was designed and simulated using cadence software as shown in fig. 4 [12]. To get the optimum bias, small-signal simulation and 1dB compression point simulation are completed by their power output capability. Resulting design values can be shown in table 2.

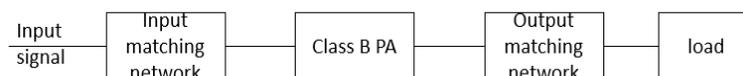


Fig. 3: Block diagram of a class B power amplifier

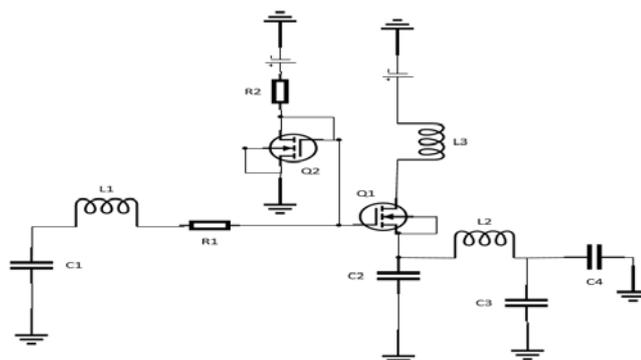


Fig. 4: PA schematic

A dual gate (cascode) architecture is used to reduce the Miller effect and also increase the breakdown voltage across the device [12]. The input LC network is matched to the operating frequency and the output LC network functions as an impedance tuning

network [2]. This approach provides maximum output power at the fundamental frequency while also providing a low load impedance at harmonic frequencies, as is required for a Class B device [12].

Table 2: 2.4GHz PA driver stage component

Parameter	Size (Unit)
Q1	W/l=4.8um/1um (f=16,m=12)
Q2	W/l=0.3um/1um
R1	14.5 Ohm
R2	13K Ohm
L1	22 nH(Q=20)
L2	15 nH (Q=20)
L3	15 nH (Q=20)
C1	200 fF
C2	10 pF
C3	10 pF
C4	10 pF

As seen in fig. 5 (a), the output power was 26 dB, PAE can reach maxim 70 % as seen in fig. 5(b), also, the total power of the PA was 6.9 mW.

As seen in fig. 6 (a), Kf was larger than 1 for all frequencies from 1 to 3 GHz, so this circuit was totally stable. And the Power gain could reach 90 dB.

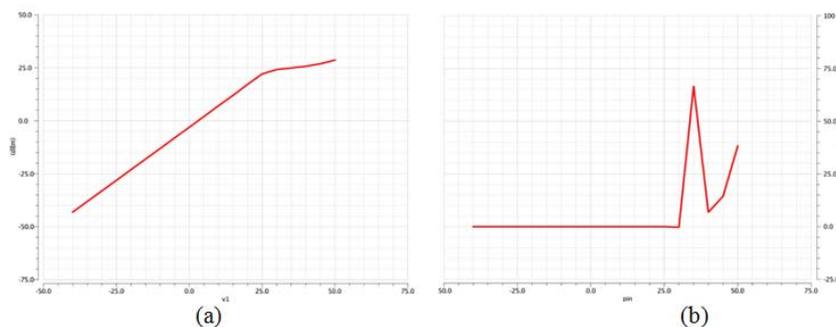


Fig. 5: (a) PA output power (b) PAE

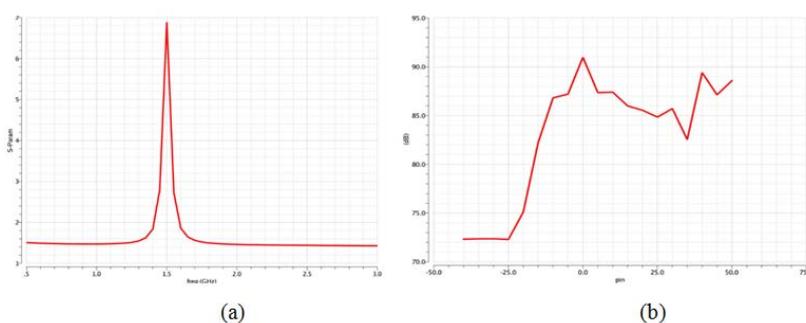


Fig. 6: (a) Kf (b) power gain

This paper describes the method of designing and simulating power amplifier using cadence software based on SIMC CMOS process 180 nm technology. This PA is used for sensor networks. This research is still in the early stages of development of a low cost and low power device. In order to reach the performance that is needed, the PA process uses group III and IV elements. This circuit meets the scheduled requirements for the CMOS process, but it still has room to improve performance metrics. When the sensor is coupled with communications technologies such as mobile phones and the Internet, the sensor network constant information flow between individuals and their doctors. Such low cost and low power device can save a lot of hospitalization resources. To realize this, future improvement is needed.

As seen the fig. 5 and 6, the design could reach the target. However, for a transmitter usually has many blocks, such as filters, ADCs, and frequency synthesizers. In order to build a complete transmitter, these blocks are not enough, and more blockers should be done. Also, more work can be done to improve the performance, such as better class B power amplifier topology. I can cover and explore more deeply on this topic if time permitted. I believe power consumption is very important for healthcare applications. In order to achieve an ultra-low power system, system and circuit design both need improvements. Secondly, since the technology nodes are becoming smaller and smaller, technology creates more challenges for analog/RF designers. For low supply voltage, it is not easy to design a very linear mixer. Besides, accurate device modeling is needed, due to the leakage and process variations.

CONFLICT OF INTERESTS

Declared none

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